Abstract of the Disclosure

A sense amplifier having a synchronous reset capability or an asynchronous reset capability, which is readily implemented and has high speed, is provided. The sense amplifier includes a first sense-amplifying unit which sense-amplifies an input signal in response to a clock signal and generates an output signal, and a second sense-amplifying unit which sense-amplifies a complementary signal of the input signal in response to the clock signal and generates a complementary signal of the output signal. The sense amplifier further includes a first controller which is connected to the first sense-amplifying unit and sets the output signal in response to a reset signal and an inverted signal of the reset signal, and a second controller which is connected to the second sense-amplifying unit and resets the complementary signal of the output signal in response to the reset signal and the inverted signal of the reset signal.

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